**Report HW 3 ECE-111**

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# **Homework 3a (Johnson Counter)**

1. **SystemVerilog design code**
   1. **johnson\_counter**

**A computer screen with colorful text

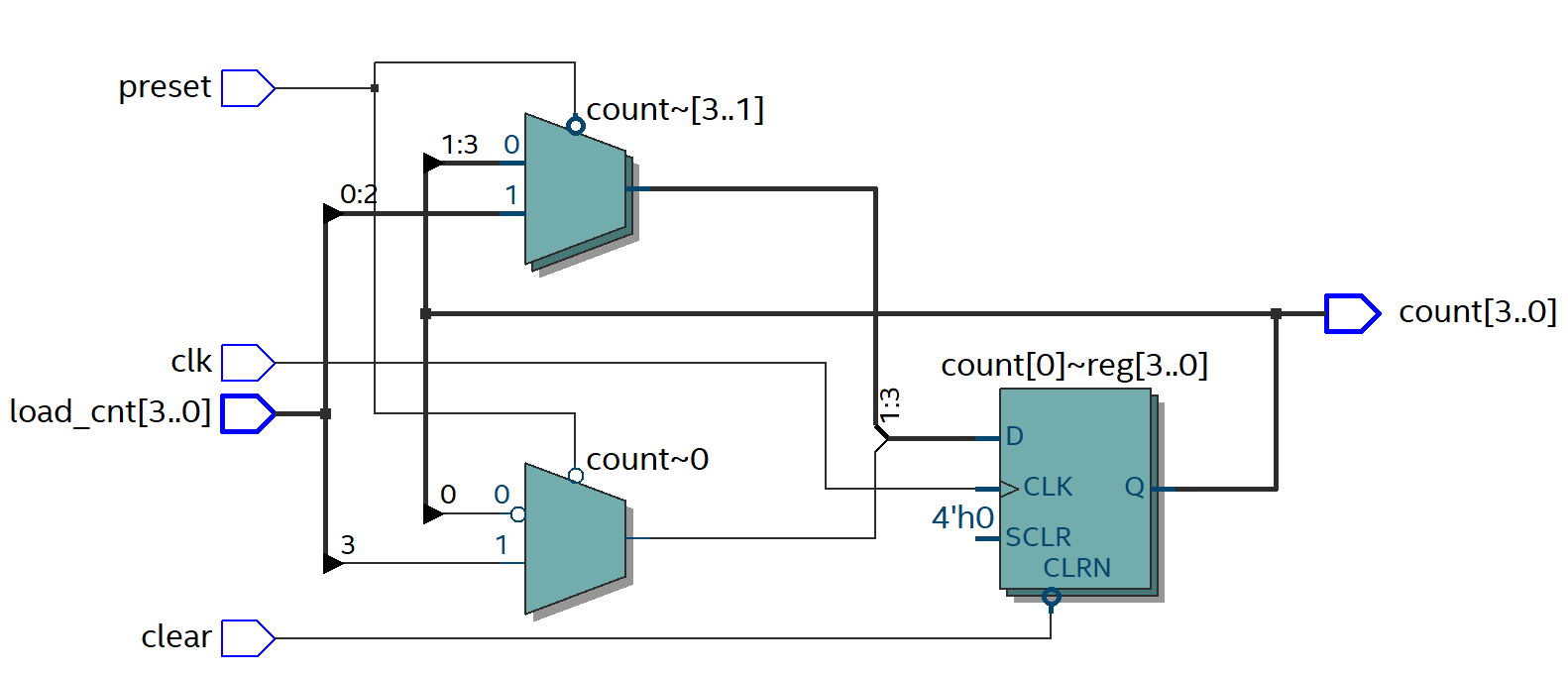
AI-generated content may be incorrect.**

1. **Synthesis Resource usage and schematic generated from RTL netlist viewer**
   1. **Resource Usage**

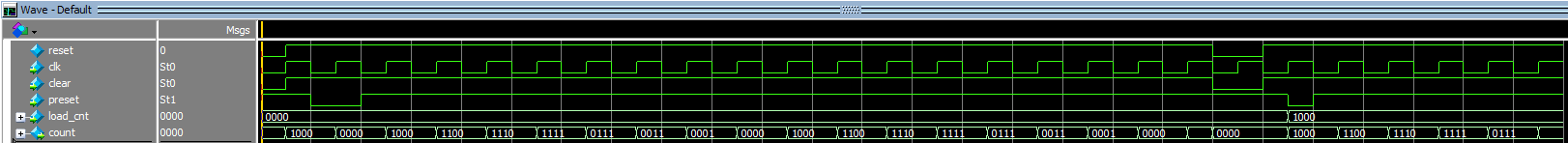
**A screenshot of a computer program

AI-generated content may be incorrect.**

* 1. **RTL netlist viewer**

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1. **Simulation snapshot and explain simulation result**

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**When reset/clear flag is low, the count is set to 0000, and when preset is low, the count is set to load\_cnt which is 0000 in the first low preset flag. After that, when the count and preset are both high, the count change from 0000 to 1000 to 1100 to 1110 to 1111 to… back to 0000, which is the expected behavior of johnson counter. When the second reset and preset flag lowered, both flag perform the same as previous, with preset to 1000.**

1. **Post-Mapping schematic**

**A diagram of a computer network

AI-generated content may be incorrect.**

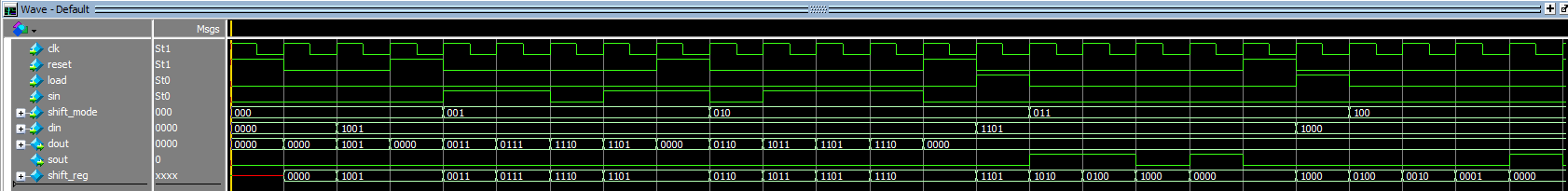
# **Homework 3b (Universal Shift Register)**

1. **SystemVerilog code snapshot**
   1. **universal\_shift\_register (student fill part)**

**A screen shot of a computer program

AI-generated content may be incorrect.**

1. **Synthesis Resource usage and schematic generated from RTL netlist viewer**
2. **Simulation snapshot and explain simulation result**



1. **Post-Mapping schematic**